AMENDMENTS TO THE SPECIFICATION

Abstract

A method and circuit for testing an IC using intelligent test vector formatting is provided. A first memory stores a test vector mask to indicate if corresponding test vector data is deterministic or random. A second memory contains a sequence of bits that represent the deterministic test vector data. A random number generator, e.g. an LFSR, generates a reproducible sequence of pseudo random bits that is based on a seed value. A selector circuit is used to select bits either from the second memory or from the LFSR based on the value of the mask vector. The output of the selector provides a fully specified test vector for application to the DUT. The LFSR can be fabricated on the DUT, thereby minimizing tester throughput and improving performance. The output of the DUT can be coupled back to stages of the LFSR, thereby increasing the effective randomness of the result.